REMARKS

The Examiner is thanked for the careful review of this Application. Claims 6, 8, and 26-35 are pending after entry of the present Amendment. Claims 1-5, 7, and 9-25 were cancelled. Certain claims were amended to better define the invention. The amendments do not introduce new matter.

Rejections under 35 U.S.C. § 103(a):

The Office has maintained the 35 U.S.C. § 103(a) rejection of claims as being unpatentable over U.S. Patent No. 6,333,255 to Sekiguchi in view of U.S. Patent No. 6,277,728 to Ahn et al. ("Ahn"). Specifically, in the Advisory Action, the Office states that while the two inside lines 17 are in direct contact with the source/drain regions, the two inside lines 17 are not electrically in contact with the metallization lines and vias.

First, the Applicants draw the Office's attention to amendments made to independent claims 6, 28, and 34. For instance, independent claim 6 has been amended to specifically recite that each of the supporting stubs is configured to form a supporting column that extends from the passivation layer formed over a dielectric layer defined over the transistor devices through the plurality of interconnect levels. Furthermore, as amended, the plurality of supporting stubs are not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias. In the same manner, independent claims 28 and 34 have been amended to recite that the semiconductor device also includes an intermetal dielectric layer (ILD) as well as a passivation layer formed thereon. Given the amendments to independent claims 6, 28, and 34 and at least the following reasons, the Applicants respectfully request that 103(a) rejection of claims be withdrawn.

It is respectfully submitted that Sekiguchi's multilevel structure implementing gas-dielectric in view of the multilevel interconnect structure having an outer low-K dielectric coating, as shown in Ahn, fails to teach or suggest all the features of the claimed invention. Contrary to the Office' assertion, the two inside "lines" as well as the two outside lines (reference number 17) shown in Sekiguchi are wires, and as wires, enable flow of current between the multiple levels of the semiconductor structure and thus provide electrical connection. Specifically, the wires are formed directly over the source/drain regions of Sekiguchi as shown in Figures l(a)-9.

As amended, in the claimed invention, each of the supporting stubs forms a supporting column that is disposed over the passivation layer, and not the source/drain region. In the specification of the subject application, the Applicants specifically state that the stubs are formed in the interlevel dielectric layer down to the passivation layer. As such, the stubs of the claimed invention provide mechanical functionality so as to reinforce the structure of the multilevel structure and do not have any electrical functionality. See page 12, lines 19-21. As such, this is in contrast to the two inside lines 17, which as acknowledged by the Office in the Advisory Action, are in direct contact with the source/drain region, and thus, may be electrically functional.

Furthermore, Sekiguchi and Ahn fail to teach forming of an ILD layer over the substrate surface and the transistor devices, and a passivation layer formed over the ILD layer, as defined in amended independent claims 28 and 34. In the claimed invention, the material of the ILD layer is a substantially robust material and is used so as to provide ample insulation. In the same manner, the passivation layer is used to protect the active components on the substrate from corrosion and chemical reactions during the fabrication process. Neither Sekiguchi nor Ahn use or suggest using an ILD layer and passivation layer, as defined in independent claims 28 and 34.

Even if the porous low-K dielectric of Ahn were to be used in the multilevel structure of Sekiguchi, one of ordinary skill in the art would not have arrived at the claimed invention. Specifically, Sekiguchi uses either a carbon insulating layer or silicon dioxide layer and lower and upper silicon dioxide layers as stoppers, or silicon dioxide layer as an insulating layer and silicon nitride lower and upper layers as stoppers. The insulating layers are etched and depending on the embodiment, the multilevel structure is either filled with the gas generated as a result of the oxygen plasma or low-K dielectric constant material. That is, while the carbon insulating layers or the silicon dioxide layers of the multilevel structure are etched in all of the embodiments of Sekiguchi, all the upper and lower silicon dioxide or silicon nitride layers are remained intact after the etch processes so as to provide and maintain the structural integrity of the multilevel semiconductor device. In short, even if the porous low-K dielectric material of Ahn were to be used in the multilevel structure of Sekiguchi, the modified multilevel structure would not be the same as the semiconductor device of the subject invention. The modified multilevel structure would still include all the upper and lower silicon dioxide or silicon nitride insulators in addiction to the porous low-K dielectric formed around the interconnect lines, trenches, and vias. As a result, the modified

multilevel structure of Sekiguchi would have a higher dielectric constant than the semiconductor of the claimed invention wherein the interconnect metallization lines and conductive vias are isolated by porous dielectric material.

Yet further, neither Sekiguchi nor Ahn teach using a multilevel structure where an ILD layer and a passivation layer are formed over the transistor devices (as defined in independent claims 28 and 34) so as to prevent any potential damage to the transistor devices. In Sekiguchi, upper and lower silicon dioxide layers silicon nitride layers are used to maintain and provide the integrity of the structure. However, such modifications has not been taught or suggested in either Sekiguchi or Ahn.

Accordingly, for at least the above-stated reasons, independent claims 6, 28, and 34, are patentable under 35 U.S.C. § 103(a) over Sekiguchi in view of Ahn. Claims 8, 26, and 27, 29-32, and 35, each of which ultimately depends from the applicable independent claim 6, 28, and 34 are likewise patentable under 35 U.S.C. § 103(a) over Sekiguchi in view of Ahn for at least the same reasons set forth for the applicable independent claim.

In view of the foregoing, the Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6913. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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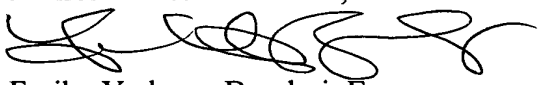

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